Cryogenic Small-Signal Model for 0.55-μm Gate-Length Ion-Implanted GaAs MESFET's

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***Abstract*—The cryogenic microwave performance of 0.5 x 300-μm gate ion-implanted GaAs MESFET's are presented. The devices studied here have been fabricated as part of a process control monitor chip (PCM) which uses comparable industry standard design rules. We have performed detailed small-signal element modeling to determine the temperature dependence of important physical parameters over a lattice temperature range from 300 K to 115 K. We find appreciable improvement in cut-off frequency and well behaved temperature dependence of transconductance (g_m) and gate-source capacitance (C_{gs}). Empirical relations for the temperature dependence of f_T, $f_{\max}$, g_m, and C_{gs} that should provide accurate temperature dependant device and circuit models, are presented.**

I. Introduction

THE ABILITY to selectively implant planar devices and integrated circuits, combined with excellent uniformity, high throughput, and low cost, makes ion implantation the most cost-effective technology choice for large scale manufacturing of monolithic microwave integrated circuits (MMIC's) and digital integrated circuits. In 1984, Feng *et al.* [1] reported a noise figure of 2.8 dB with 8.3-dB associated gain at 30 GHz and a gain of 6 dB at 60 GHz. However, the speed and noise performance of high-electron mobility transistors (HEMT's) was superior mainly due to the factor of two higher current-gain cutoff frequency (f_T) of HEMT's over GaAs MESFET's from 1984 to 1988. In 1990, the experimental evidence that f_T values equal to or greater than those achieved with HEMT's and pseudomorphic-HEMT's (P-HEMT's) can also be achieved by ion-implanted GaAs and InGaAs MESFET's was presented [2]. These measured f_T results clearly suggest that the average electron velocity under the gate is determined primarily by the high-field electron velocity rather than the low-field electron mobility. Hence, one must conclude that the transport properties of the two-dimensional electron gas (2-D EG) in HEMT's and P-HEMT's do not make a significant contribution to the high-frequency and high-speed performance of these devices. Further experimental evidence was provided in 1991 when it was demonstrated that the change of f_T as a function of temperature on HEMT's and MESFET's is similar over a temperature range from 300 K to 110 K proving that the high-field electron velocity controls transport in GaAs based field-effect transistors [3]. For practical applications it is necessary to accurately model the temperature behavior of discrete devices that are then used to predict circuit behavior over a comparable temperature range. In this letter, we provide an accurate temperature dependant model of the parameters derived from the transistor scattering (s) parameters as a function of temperature: transconductance (g_m), gate-source capacitance (C_{gs}), drain-gate capacitance (C_{dg}), current-gain cut-off frequency (f_T), and maximum frequency of oscillation ($f_{\max}$).

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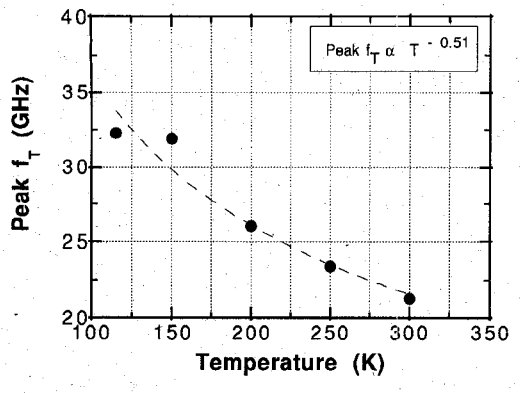
II. Device Structure and Fabrication

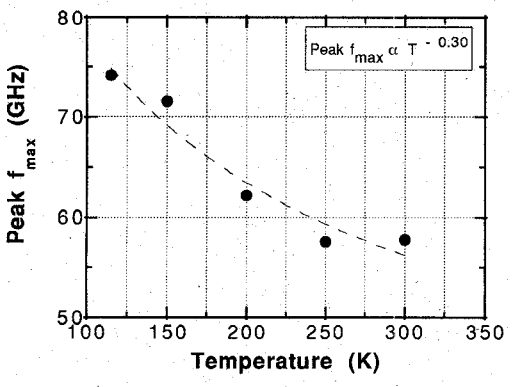
The process control monitor GaAs MESFET uses selective planar ion implantation and a photolithography defined 0.55 μm x 300 μm gate. The n^+ drain and source implants were formed with 1 x 10^{13} cm^{-2} Si with a 150 keV dose. The n-channel implant was formed with 6 x 10^{12} cm^{-2} Si with a 100 keV dose. The gate is recessed to improve transconductance and reduce surface effects, while also providing adjustment to the pinch-off voltage and saturation current. The drain to source spacing is 3 μm and the gate to source spacing is 1 μm. The gate is composed of six fingers with each finger having a 50-μm width. Typical f_T across a 3-inch wafer is 20 GHz.

III. Results

The two-port microwave s-parameters were collected from 0.5 to 26.5 GHz using a Hewlett-Packard 8510 B network analyzer. On-wafer measurements have been made at 300 K using a Cascade model 42 D microwave probe station and at reduced lattice temperatures using a unique cryogenic microwave probe station [4]. The electrical reference plane is established by an "off-wafer" short-open-matched load-thru calibration using an impedance standard substrate from Cascade Microtech. The lattice temperature is determined by measuring the junction characteristics of a bipolar junction transistor. The measured S-parameter data is used to calculate the maximum unilateral transducer power gain, GTUMAX, (the maximum available power gain cannot be calculated over the measured frequency range since the stability factor $K < 1$) and the forward current gain H21. The f_T and $f_{\max}$ are then determined from the gain-frequency profile and the peak f_T and $f_{\max}$ versus lattice temperature are plotted in Fig. 1(a) and (b). We find $f_T \propto T^{-0.51}$ and $f_{\max} \propto T^{-0.3}$ for the devices in this study. The technique originally proposed in [5] is then



(a)



(b)

Fig. 1. (a) Plot of the measured peak f_T versus lattice temperature with no corrections for pad parasitics. The peak f_T a T -0.51 over a temperature range from 300 K to 115 K. (b) Plot of the measured peak $f_{\max}$ versus lattice temperature. The peak $f_{\max}$ a T -0.30 over a temperature range from 300 K to 115 K.

used to determine the extrinsic g_m, C_{gs}, and at a frequency of 3 GHz. These parameters are then validated using a linear small-signal circuit simulator using the the small-signal equivalent circuit of Fig. 2. In Fig. 3, the dependence of C_{gs} with lattice temperature and bias (percentage of I_{dss}) is shown. It is found that $C_gs \propto T^{+\beta}$ where $0.13 < \beta < 0.17$ depending on bias. The behavior of C_{dg} with lattice temperature and bias is relatively insensitive to the lattice temperature. In Fig. 4, we plot the behavior of g_m versus lattice temperature and bias. We find $g_m \propto T^{-\beta}$ where $0.32 < \beta < 0.38$ depending upon the drain-source current value. In addition, the drain-source resistance (R_{ds}) decreases with decreasing temperature because of an effective larger conductive channel cross section due to enhanced carrier velocity.

IV. Discussion

It is important to accurately determine the temperature dependence of f_T, $f_{\max}$, g_m, and C_{gs}. As the lattice temperature is reduced the carrier high-field velocity increases [3], [6] thereby increasing the g_m. The metal-semiconductor barrier height increases [7] with reduced lattice temperature that increases the depletion width under the gate near the source resulting in a smaller value of C_{gs}. In addition, the larger barrier height reduces gate leakage allowing more efficient modulation of the channel charge thereby increasing the g_m.

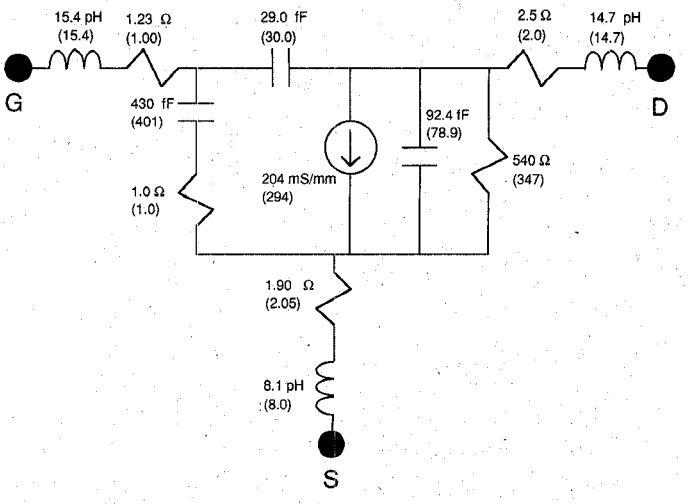


Fig. 2. Equivalent circuit used to model the measured s-parameters. Circuit element values at temperatures of 300 K (115 K) are shown, V_{ds} = 3.0 V and the device is biased at 100% of I_{dss}.

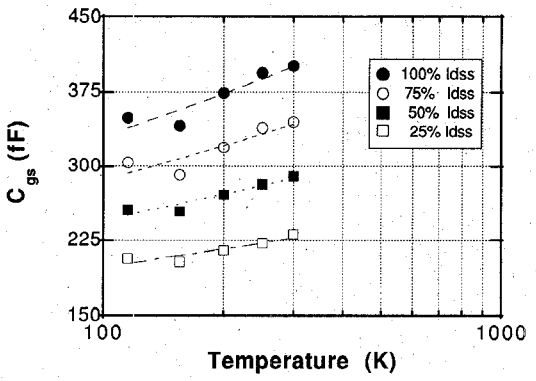


Fig. 3. Plot of the gate-source capacitance C_{gs} versus lattice temperature for V_{ds} = 3.0 V and different values of I_{ds}, where I_{dss} = 70 mA at 300 K and increases to 88 mA at 115 K. We find that $C_{gs}\alpha T^{+0.17}$ at 100% I_{dss}, $C_{gs}\alpha T^{+0.16}$ at 75% I_{dss}, $C_{gs}\alpha T^{+0.15}$ at 50% I_{dss}, and $C_{gs}\alpha T^{+0.13}$ at 25% I_{dss} over a temperature range of 300 K to 115 K.

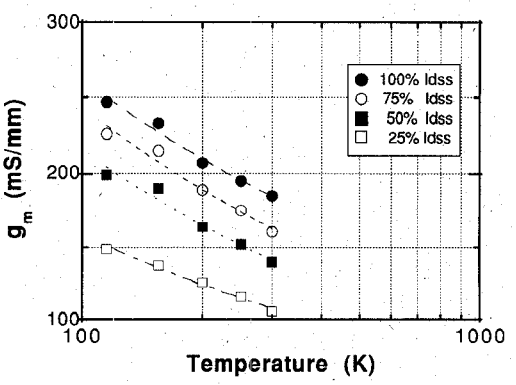


Fig. 4. Plot of the transconductance g_m versus lattice temperature for V_{ds} = 3.0 V and different values of I_{ds}, where I_{dss} = 70 mA at 300 K and increases to 88 mA at 115 K . We find that $g_m\alpha T^{-0.32}$ at 100% I_{dss}, $g_m\alpha T^{-0.37}$ at 75% I_{dss}, $g_m\alpha T^{0.38}$ at 50% I_{dss}, and $g_m\alpha T^{-0.35}$ at 25% I_{dss} over a temperature range of 300 K to 115 K.

The feedback capacitance, C_{dg}, is essentially independent of temperature, because it is dominated by fringing electric fields, and only slightly sensitive to the increased charge

accumulation from drain to gate at higher drain currents. The decrease in C_{gs} and corresponding rise in g_m results in a f_T that increases appreciably at a reduced lattice temperature, since $f_T \sim \frac{g_m}{2\pi C_g}$. The $f_{\max}$ is sensitive to both f_T and R_ds and because R_{ds} decreases with decreasing temperature the $f_{\max}$ is less sensitive to temperature than f_T. These results show that the conventional hybrid-π model can predict the small-signal behavior of GaAs based MESFET's over a wide temperature range to at least 20 GHz.

V. Summary

An empirical temperature dependant model is presented for important parameters used to estimate the microwave performance of PCM 0.5 x 300 μm-gate GaAs MESFET's. We find that $f_T \propto T^{-0.5}$, $f_{\max} \propto T^{-0.3}$, $C_{gs} \propto T^{+\beta}$ where $0.13 < \beta < 0.17$, and $g_m \propto T^{-\beta}$ where $0.32 < \beta < 0.38$. This work provides a basis for predicting discrete GaAs MESFET and GaAs MMIC performance over a temperature range from 300 K to 110 K.

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